IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Kenneth C. Hsu, et al.
Serial No.:	09/811,239
Filing Date:	March 16, 2001
Examiner:	Thomas H. Stevens
Art Unit:	2123
Title:	APPARATUS AND METHODS FOR CIRCUIT EMULATION OF A POINT-TO-POINT PROTOCOL OPERATING OVER A MULTI-PACKET LABEL SWITCHING NETWORK

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

DECLARATION PURSUANT TO 37 C.F.R. § 1.131

We, Kenneth C. Hsu and Mitri Halabi hereby declare and state that:

1. We are the inventors of the subject matter of the above-referenced Application entitled "Apparatus and Methods for Circuit Emulation of a Point-to-Point Protocol Operating over a Multi-Packet Label Switching Network" filed on March 16, 2001 (the "Application").

2. The Examiner rejected Claims 1-24 of the Application in an Office Action dated June 7, 2004 based, in whole or in part, on a Network Working Group Internet Draft paper entitled "SONET/SDH Circuit Emulation Service Over MPLS (CEM) Encapsulation" by Malis, et al. published February 2001 (the "Malis, et al. paper"), less than one year prior to the effective filing date of the Application..

3. We developed an understanding and appreciation of the subject matter of at least Claims 1-24 of the Application prior to February 2001, the publication date of the Malis, et al. paper, while working at Vivace Networks, Inc., now Tellabs San Jose, Inc. Prior to February 2001, we prepared a document entitled "SONET Circuit Emulation Point-to-Point Protocol over MPLS Network" containing a description of the subject matter of Claims 1-24 of the Application. Attached herewith as Exhibit A is a redacted version of the document showing pertinent portions detailing our understanding of the subject matter of the claims. This document demonstrates that we had a clear comprehension of the invention, its components, and their interrelationships prior to the publication date of the Malis, et al. paper.

4. Prior to the publication date of the Malis, et al. paper, with the help of a patent attorney, we generated a draft of the Application that, prior to the publication date, was substantially identical to and included all of the subject matter of the Application as filed.

5. Between the publication date of the Malis, et al. paper and the filing date of the Application, we finalized the paperwork in anticipation of filing. Attached herewith AS Exhibit B our correspondence papers with dates redacted demonstrating some of our continuing activities, which began prior to the publication date of the Malis, et al. article and continued through to the filing date of the Application.

5. We hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. Further, I declare that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Application or any patent issuing thereon.

Signed this _____ day of November, 2004.

_____

Kenneth C. Hsu

Signed this _____ day of November, 2004.

_____

Mitri Halabi

5. We hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. Further, I declare that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Application or any patent issuing thereon.

Signed this 3rd day of November, 2004.

Kenneth C. Hsu

Signed this _____ day of November, 2004.

Mitri Halabi

5. We hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and b elief are believed to be true. Further, I declare that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Cod e, and that such willful false statements may jeopardize the validity of the Application or any patent issuing thereon.

Signed this _____ day of November, 2004.

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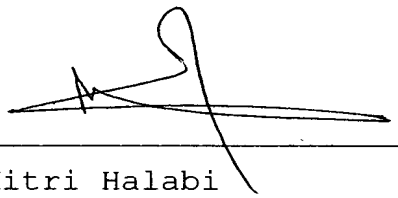
Kenneth C. Hsu

Signed this 8th day of November, 2004.



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Re: Draft Patent Application
Entitled: **APPARATUS AND METHODS FOR CIRCUIT EMULATION OF A POINT-TO-POINT PROTOCOL OPERATING OVER A MULTI-PROTOCOL LABEL SWITCHING NETWORK**
Inventors: Hsu
Our Ref.: 10386-0007-999

Dear Mr. Hsu:

Enclosed is a draft of the above-referenced patent application for your review. Please review the draft to ensure that: (1) it is accurate and complete; (2) it sets forth sufficient detail to enable those skilled in the art to build and use the invention; and (3) the best mode of practicing the invention, i.e., the preferred way of constructing and using the invention is disclosed.

It is very important that we include a complete and accurate description of your invention in the application at the time of filing since an attempt to add new matter to clarify or further describe the invention will almost certainly result in the loss of the benefit of the original filing date and will require the filing of another application. Accordingly, if you currently have plans to modify and improve the invention or add features to the invention that are not disclosed in the draft application, these features need to be added to the patent application at this time. Furthermore, if there are any details regarding the construction and use of the invention that are not generally known, we must disclose them.

We wish to verify at this time the appropriate list of inventors (including their home addresses and citizenship information). Under the law, an inventor is anyone who contributes to the subject matter of one or more claims in the patent application. Please discuss with us any questions that you have in connection with inventorship.

Patent Office regulations require that we identify any prior art that may show or suggest the claimed invention. Accordingly, please provide us with any patents, publications, or product literature that you believe is relevant to the invention and which you have not already disclosed to us. Please note that this duty of disclosure exists throughout the pendency of the patent application.

Please call to set up an appointment with me when you are ready to discuss various marked areas in the draft application where we need to include more detailed information or clarification.

If you have any questions or concerns, please do not hesitate to contact me.

Very truly yours,

Roxana Hwu Yang

Enclosures

cc: Mitri Halabi (w/ encls)
Frank E. Morris (w/o encls)

System Specification

SONET Circuit Emulation Point-to-Point Protocol over MPLS Network

Doc. No 030-xxxxx-0001
Rev 0.6

[redacted]

Approvals	Date
President	
V.P. Engineering	
Marketing	
Operations	
Sales	

Revision History

Rev	Author	Date	Description
0.0	Ken Hsu	[redacted]	Draft
0.1	Ken Hsu	[redacted]	Changed per Mitri's comments
0.2	Ken Hsu	[redacted]	Changed to use packet parser data format
0.3	Ken Hsu	[redacted]	Added pin description, register map, and programmer guide
0.4	Ken Hsu	[redacted]	Remove DS3, added quad OC-3, and CDVT DRAM
0.5	Ken Hsu	[redacted]	Changed encapsulation and others per Mitri's comments
0.6	Ken Hsu	[redacted]	Changed TDM header per CEM draft

CONTENTS

1. INTRODUCTION 5

1.1 PURPOSE 5
1.2 SCOPE 5
1.3 ACRONYMS 5
1.4 REFERENCES 6

2. OVERVIEW 7

2.1 SONET RATES AND FORMATS 7
2.2 SONET LINE INTERFACE CARDS 8
2.2.1 Single OC-48 I/F Module 8
2.2.2 Quad OC-12 I/F Module 9
FIGURE 2-3. QUAD OC-12 INTERFACE MODULE 10
2.2.3 Quad OC-3 I/F Module 10
FIGURE 2-4. QUAD OC-3 INTERFACE MODULE 10
2.3 TIMING MODELS 11
2.4 FREQUENCY JUSTIFICATION 11
2.5 PAYLOAD POINTER 12

3. ENCAPSULATION 14

3.1 TDM PACKETS 14
3.2 HDLC-LIKE PPP PACKET 15
3.3 PAYLOAD CAPACITY AND RATE 16
3.3.1 Emulate STS Circuits 16
3.3.2 Example 17
3.3.3 Summary 17

4. OPERATIONS 19

4.1 BLOCK DIAGRAM 19
4.2 FUNCTIONAL DESCRIPTION 20
4.2.1 Incoming Parallel Telecom Bus 20
4.2.2 Input Telecom Bus Interface (ITCBI) 22
4.2.3 Drop Telecom Bus Interface (DTCBI) 24
4.2.4 Input TDM Channel FIFO (INTCF) 24
4.2.5 POS Level-3 Input Interface (INPHY) 24
4.2.6 Receive Circuit Emulation Processor (RCEP) 24
4.2.7 Receive TDM Channel FIFO (RXTCF) 24
4.2.8 POS Level-3 Receive Interface (RXPHY) 25
4.2.9 POS Level-3 Transmit Interface (TXPHY) 25
4.2.10 Transmit TDM Channel FIFO (TXTCF) 26
4.2.11 Transmit Circuit Emulation Processor (TCEP) 26
4.2.12 Output TDM Channel FIFO (OUTTCF) 27
4.2.13 POS Level-3 Output Interface (OUTPHY) 27
4.2.14 Add Telecom Bus Interface (ATCBI) 27
4.2.15 Output Telecom Bus Interface (OTCBI) 27
4.3 CIRCUIT EMULATION PROCESSOR 28

4.3.1 Receive Channel Transfer Controller (RCTC) *29*
4.3.2 Channel Diagnostic Loopback (CHNDLP) *31*
4.3.3 Receive Channel Elastic Store (RCES) *31*
4.3.4 Receive Adaptation Layer Processor (RALP) *32*
4.3.5 Channel System-side Loopback (CHNSLP) *33*
4.3.6 Transmit Adaptation Layer Processor (TALP) *33*
FIGURE 4-9. FRAME SYNCHRONIZATION STATE DIAGRAM 35
4.3.7 Transmit Channel Reassembly Memory (TCRAM) *36*
4.3.8 Transmit Channel Elastic Store (TCES) *38*
4.3.9 Transmit Channel Transfer Controller (TCTC) *40*
4.4 LOOPBACK CONFIGURATION 41
4.4.1 Loopback Toward Line Interface *42*
4.4.2 Loopback Toward POS-PHY Interface *43*
4.5 PACKET DELAY VARIATION AND TOLERANCE (PDVT) 44
4.5.1 Intrinsic PDV *44*
4.5.2 PDV Tolerance (PDVT) *45*

5. PIN DESCRIPTION 47

5.1 RECEIVE POS LEVEL-3 INTERFACE SIGNALS 47
5.2 TRANSMIT POS LEVEL-3 INTERFACE SIGNALS 48
5.3 OUTPUT POS LEVEL-3 INTERFACE SIGNALS 51
5.4 INPUT POS LEVEL-3 INTERFACE SIGNALS 53
5.5 OUTPUT TELECOM BUS INTERFACE SIGNALS 55
5.6 INPUT TELECOM BUS INTERFACE SIGNALS 56
5.7 DROP TELECOM BUS INTERFACE SIGNALS 58
5.8 ADD TELECOM BUS INTERFACE SIGNALS 59
5.9 MICROPROCESSOR (CPU) INTERFACE SIGNALS 60
5.10 RAM INTERFACE SIGNALS 61
5.11 JTAG TEST ACCESS PORT 62
5.12 GENERAL 63

1. INTRODUCTION

1.1 Purpose

This document provides an overview of technical requirements for transporting time division multiplexed (TDM) digital signals over a packet-oriented multi-protocol label switching (MPLS) network. The transmission system for circuit-oriented TDM signals is synchronous optical network (SONET). To support the TDM traffic, which includes voice, data and private leased line service, MPLS network must emulate the circuit characteristics of SONET payloads. HDLC-like point-to-point protocol (PPP) and MPLS shim header are used to encapsulate TDM signals and provide the circuit emulation service (CES).

The objective of this document is to examine the synchronization criteria of the SONET transmission system, define TDM segmentation and reassembly (SAR) functions that meet the criteria, and resolve encapsulation issues, such as packet overhead and payload sizes, regarding CES over MPLS network.

1.2 Scope

The architecture described in this document will be used as the basis for the development of a TDM SAR. The TDM SAR provides CES over MPLS network for the following digital signals.

1) STS-1 synchronous payload envelop (SPE)

2) STS-Nc SPE (N = 3, 12, or 48)

Other SONET signals, such as virtual tributary (VT) structured sub-rate mapping, are not supported. Since encapsulated TDM packets are transported on an OC-192c line, highest SONET signals supported is STS-48c.

This document illustrates the functional requirements of the TDM SAR chip. Some design details, such as I/O pin designation, memory/register arrangement, and timing analysis, may be included. They are for references only. Actual chip design is beyond the scope of this document.

1.3 Acronyms

See "Technical Word List." [10]

1.4 References

[1] "SONET Basic Description including Multiplex Structure, Rates, and Formats", ANSI T1.105, October 1995
[2] "SONET – Payload Mappings", ANSI T1.105.02, May 1995
[3] "Circuit Emulation Service Interoperability Specification", ATM Forum af-vtoa-0078.000 V2.0, January 1997
[4] "Packet Over SONET Interface Specification for Physical Layer Devices – POS-PHY Level 3", PMC Compatibility Specification PM-980495 Issue 3, November 1998
[5] "Mapping Point-to-Point Protocol Over the Entire SONET/SDH SPE or Over Sub-rate Tributary SPE's", PMC Application Note PM-960725 Preliminary Issue 1, June 1996
[6] "AAL1 Segmentation and Reassembly Process-32", PMC PM73122 Data Sheet Issue 4, January 2000
[7] "SONET/SDH Payload Extractor/Aligner for 2488 Mbit/s", PMC PM5315 SPECTRA-2488 Data Sheet Issue 1, November 1999
[8] "Multi-service Access Device for Channelized Interface", PMC PM7390 S/UNI MACH48 Data Sheet Issue 2, December 1999
[9] "PP ASIC Data Formats", Vivace Networks, Inc. Rev 0.9, January 2000
[10] "Technical Word List", Vivace Networks, Inc. Rev 0, August 1999
[11] "ATM User-Network Interface Specification". ATM Forum V3.1, October 1995
[12] "PPP Over SONET/SDH". IETF RFC 1619, May 1994
[13] "PPP in HDLC-like Framing". IETF RF C1662, July 1994
[14] "Digital Hierarchy – Formats Specifications". ANSI T1.107, 1995
[15] "Digital Hierarchy – Supplement to Formats Specifications (DS3 Format Applications)". ANSI T1.107a, 1990
[16] "ATM Adaptation Layer for CBR Services Functionality and Specification". ANSI T1.630, August 1993
[17] "Quad SONET/SDH Payload Extractor/Aligner 155 Mbit/s", PMC PM5316 SPECTRA-4X155 Data Sheet Issue 1, Rev. 2.1, January 2000
[18] "Proposal for work plan item to support Voice over MPLS", MPLS Forum 2000.004, June 2000
[19] "Transport of Layer 2 Frames Over MPLS", IETF Internet Draft draft-martini-12circuit-trans-mpls-01.txt, May 2000

2. OVERVIEW

2.1 SONET Rates and Formats

The basic SONET modular signal is the synchronous transport signal-level 1 (STS-1). A number of STS-1s may be multiplexed into higher-level signals denoted as STS-N with N synchronous payload envelopes (SPEs). The optical counterpart of the STS-N is the optical carrier-level N or OC-N. Table 2-1 lists standard SONET line rates supported in this document.

OC Level	OC-1	OC-3	OC-12	OC-48	OC-192
SDH Term	-	STM-1	STM-4	STM-16	STM-64
Line Rate (Mb/s)	51.840	155.520	622.080	2,488.320	9,953.280

Table 2-1. Standard SONET Line Rates

Each SONET frame is 125 μs and consists of nine rows. An STS-N frame has nine rows and N*90 columns. Of the N*90 columns, the first N*3 columns are transport overhead and the other N*87 columns are SPEs. A number of STS-1s may also be linked together to form a super-rate signal with only one SPE. The optical super-rate signal is denoted as OC-Nc, which has a higher payload capacity than OC-N.

The first 9-byte column of each SPE is the path overhead (POH) and the remaining columns form the payload capacity with fixed stuff (STS-Nc only). Figure 2-1 shows an STS-1 or STS-Nc frame.

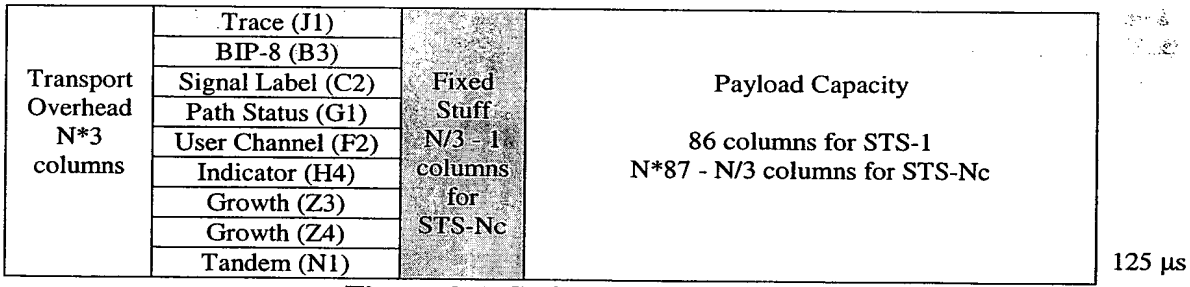

Figure 2-1. STS-1 or STS-Nc Frame

The POH of an STS-1 or STS-Nc is always nine bytes in nine rows. The payload capacity of an STS-1 (no fixed stuff) is 774 bytes per frame. The payload capacity of an STS-3c is (3*87 – 1)*9 = 2,340 bytes per frame. There is no fixed stuff for an STS-3c either. The payload capacity (without fixed stuff) of a concatenated STS-Nc, where N > 3, has (N*87 – N/3)*9 bytes. For instance, the payload capacity of an STS-192c is 149,760 bytes, which is exactly 64 times bigger than the STS-3c's. The fixed stuff (shaded area) of an STS-192c is 63*9 = 567 bytes.

There are 8,000 SONET frames per second. Therefore, the SPE size, POH plus payload capacity, of an STS-1 is 783*8*8,000 = 50.112 Mb/s. The SPE size of a concatenated STS-3c is 2,349 bytes per frame or 150.336 Mb/s. The payload capacity of an STS-192c

has 149,760 bytes per frame, which is equivalent to 9,584.640 Mb/s. Table 2-2 lists the SPE and payload rates supported.

STS Level	STS-1	STS-3c	STS-12c	STS-48c	STS-192c
Payload Size (Bytes)	774	2,340	9,360	37,440	149,760
Payload Rate (Mb/s)	49.536	149.760	599.040	2,396.160	9,584.640
SPE Size (Bytes)	783	2,349	9,396	37,584	-
SPE Rate (Mb/s)	50.112	150.336	601.344	2,405.376	-

Table 2-2. Payload Size and Rate

Different services (TDM, ATM, PPP over SONET, etc.) are mapped into STS payloads differently. The STS path signal label (C2 byte in POH) indicates the construction and content of the STS SPE. Table 2-3 listed the C2 assignments that are supported.

Byte C2 Code (Hex)	Construction and Content of the STS SPE
00	Unequipped
01	Equipped – Non Specific Payload
13	Mapping for ATM
CF	Point-to-Point Protocol over SONET

Table 2-3. C2 Assignments Supported

In TDM service (circuit emulation), the entire SPE of a lower STS level is encapsulated into PPP packets and transported in the payload area of a higher STS level. Services other than TDM are supported through a PMC multi-service chip[8].

2.2 SONET Line Interface Cards

The first product release supports two types of line cards: 10 Gb/s trunk I/F and 4 * 2.5 Gb/s port I/F. The trunk I/F card uses a single OC-192c for interfacing with the MPLS network. The OC-192c trunk I/F card is connected to the Vivace packet parser (PP) chip through a 128-bit POS-PHY type bus.

The port I/F card has four plug-in modules and each plug-in module may have one of the three SONET line interface types: single OC-48, quad OC-12, and quad OC-3. There is one TDM SAR on each I/F module. Four modules, with combined rates up to 10 Gb/s, may be connected to the PP chip through four sets of 32-bit POS-PHY level 3 buses.

2.2.1 Single OC-48 I/F Module

A single OC-48 I/F module consists of a PM5315 SPECTRA-2488 payload aligner[7], a PM7390 MACH-48 channelized multi-service access device[8], and a TDM circuit emulation SAR. The TDM SAR lies between the PMC chips and the Vivace PP chip. It performs circuit emulation on selected STS channels. The TDM SAR also adds/drops non-TDM traffic from/to the PM7390. The PM7390 interfaces with the PM5315 and PP chip indirectly via the TDM SAR

The PM5315 is configured to the single STS-48 mode. In this mode, it supports a duplex 16-bit 155.52 MHz differential PECL line-side interface for direct connection to external clock circuitry and optical transceivers. Figure 2-2 shows the I/F module.

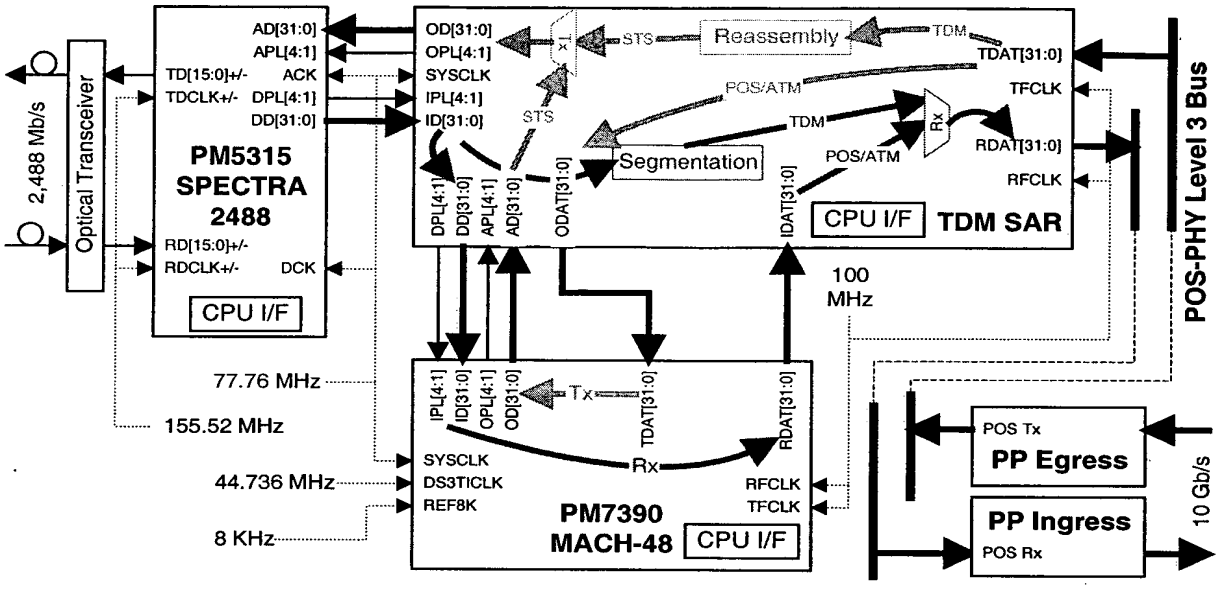

Figure 2-2. Single OC-48 Interface Module

The PM5315 interfaces electrical optical components in the line-side and performs SONET section, line, and path termination. In the system-side, it supports a 32-bit 77.76 MHz telecom bus (TCB) directly connected to the TDM SAR.

The PM7390 MACH-48 is an ATM and packet processor. It implements the ATM Forum UNI[11], PPP over SONET[12,13], and ANSI T1.107[14,15] (for DS3) specifications. The chip provides programmable assignment of STS-1 timeslots to arbitrary DS3, STS-1, STS-3c, STS-12c, or STS-48c channels. PM7390 has a 32-bit 77.76 MHz TCB line-side and 32-bit 100 MHz POS-PHY Level 3 system-side interfaces.

The TDM SAR chip provides independent time-slot interchange blocks on the incoming and out going TCB interfaces to allow arbitrary arrangement of timeslots at STS-1 granularity. The SAR has two 32-bit TCBs, one for PM5315 and the other for PM7390, and two POS-PHY Level 3 interfaces, one for PM7390 and the other for the PP chip.

2.2.2 Quad OC-12 I/F Module

The quad OC-12 I/F module consists of a PM5315, a PM7390, and a TDM SAR. The PM5315 is configured to support four duplex 8-bit 77.76 MHz TTL compatible line-side interfaces. In the system side of the PM5315, the 32-bit 77.76 MHz TCB is broken down into four 8-bit TCBs, each carrying a byte-interleaved OC-12 stream. The line-side interfaces of TDM SAR and PM7390 are configured to support four 8-bit TCBs also. Figure 2-3 shows the I/F module.

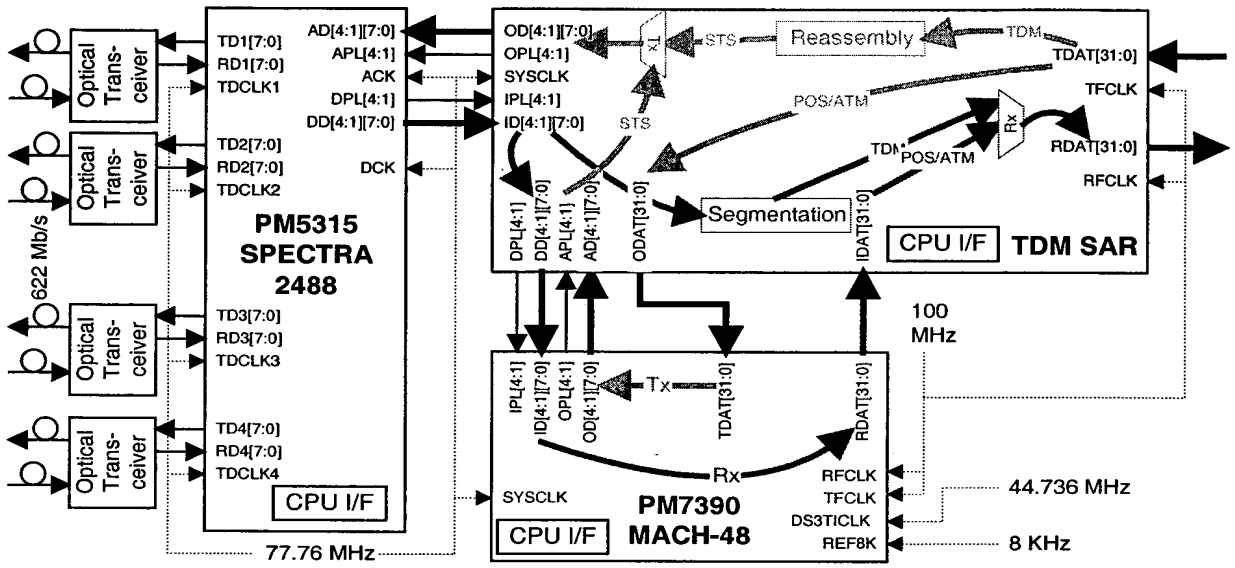

Figure 2-3. Quad OC-12 Interface Module

2.2.3 Quad OC-3 I/F Module

The quad OC-3 I/F module uses a PM5316 SPECTRA-4X155[17] instead of the 2.5 Gb/s PM5315. The 622 Mb/s PM5316 is configured to support four 155.52 Mb/s differential PECL line-side interfaces. In the system side of the PM5316, a single 8-bit 77.76 MHz TCB, carrying byte-interleaved OC-12 stream, is used. The other three TCBs are forced to low. The line-side interfaces of TDM SAR and PM7390 are configured to support only the first of the four 8-bit TCBs. Figure 2-4 shows the I/F module.

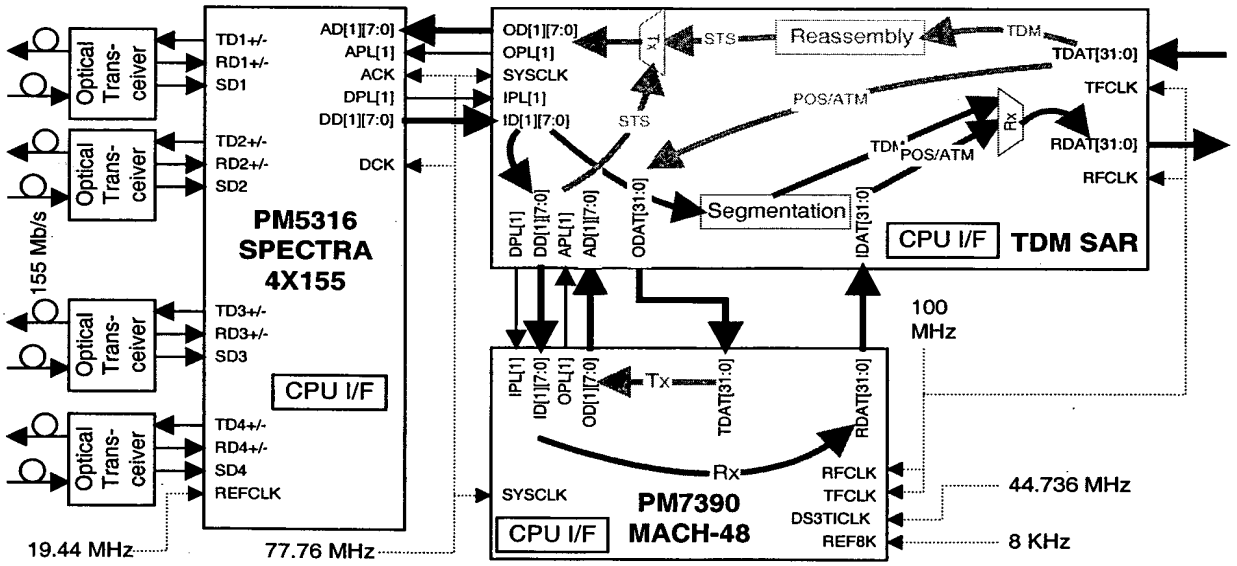

Figure 2-4. Quad OC-3 Interface Module

2.3 Timing Models

SONET network elements (NEs) are required to have an internal clock of ± 20 ppm minimum free-run accuracy. The free-running clock may be synchronized with network clock using one of four timing modes: external, through, loop, or line. Figure 2-5 illustrates the four timing modes.

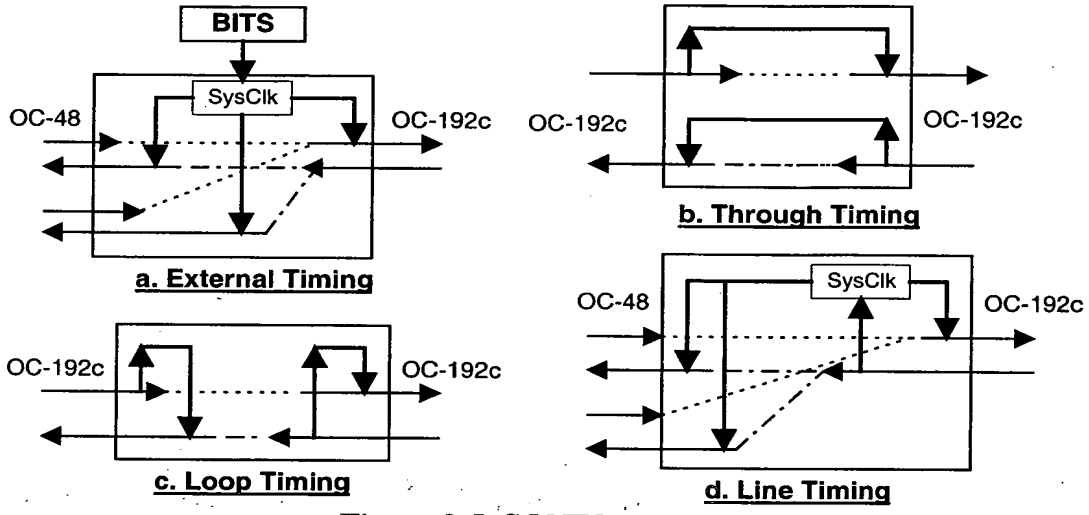

Figure 2-5. SONET Timing Modes

External timing, as shown in Figure 2-5a, from a building integrated timing supply (BITS) is the preferred mode of synchronizing SONET NEs. However, it might not be possible to synchronize the entire MPLS network with a stratum-3 (or better) BITS clock. If a BITS clock is not available, then a selected reference clock received from one of the SONET lines (Figure 2-5d) shall be used for edge switches with circuit emulation application. For intermediate switches, through timing or loop timing may also be used.

2.4 Frequency Justification

If there is a frequency offset between the frame rate of the transport overhead and that of the STS SPE, then the alignment of the SPE shall periodically slip back or advance in time through positive or negative stuffing. The stuffing activity takes place in SPECTRA when a positive or negative justification event (PJE or NJE), marked by the APL signal, is received from the TDM SAR. In drop operation, DPL signals from SPECTRA are used by both TDM SAR and MACH-48 to identify PJEs and NJEs for frequency justification.

Within MACH-48, the 77.76 MHz system clock (SYSCLK) is decoupled from 100 MHz POS-PHY clocks (RFCLK and TFCLK) through decoupling FIFOs in ATM and POS applications. In the DS3 application, elastic stores provide compensations for frequency differences between 44.736 MHz DS-3 streams and the system clock. For ATM with DS3 PLCP framing, the 8 KHz REF8K clock is used to lock PLCP frames.

For the application of circuit emulation over MPLS network, two timing modes are used in the TDM SAR: synchronized and adaptive. Figure 2-5 illustrates the two frequency justification methods.

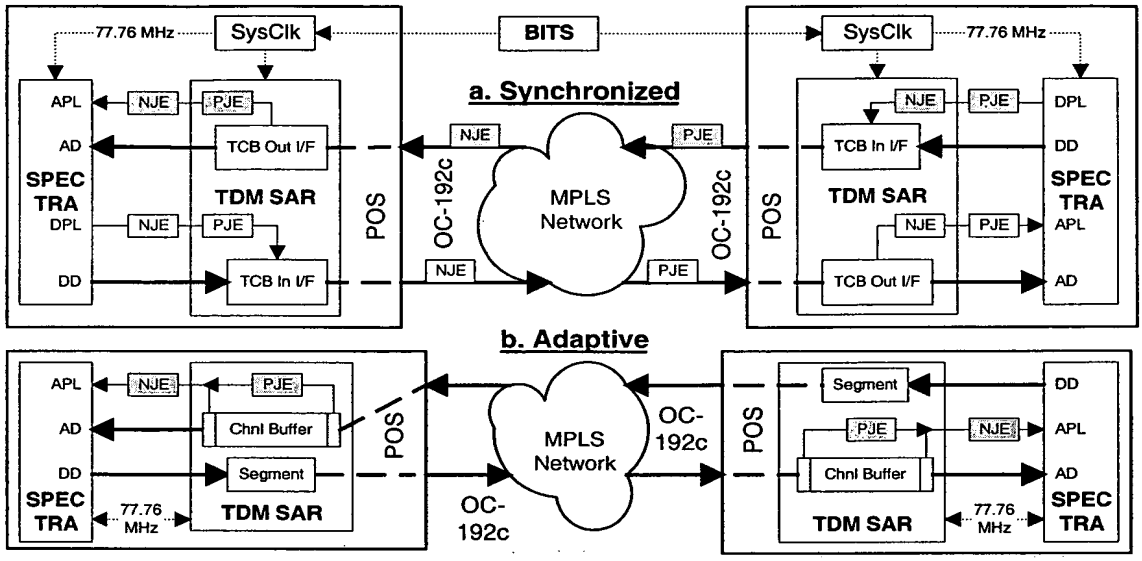

Figure 2-6. Circuit Emulation Over MPLS Network

In synchronized mode, the edge switches are synchronized with the BITS clock. The positive and negative justification events (PJE and NJE) from local SPECTRA are carried over POS to the far-end TDM SAR. The TCB output interface block in the far-end SAR plays out the justification events to properly align SPEs in transmit SONET frames.

In adaptive mode, the system clocks in edge switches are not synchronized. Frequency offset of an STS channel is compensated through locally generated NJEs and PJEs based on the average depth of the channel buffer. If the average buffer depth is increasing, then the TDM SAR issues NJEs to SPECTRA to speed up the transmission of data bytes. If the buffer depth is decreasing, then PJEs are sent to SPECTRA to insert positive stuff bytes and slow down the transmission rate.

2.5 Payload Pointer

The STS-1 payload pointer allows each SPE to float within the STS frame. Thus, the differences in phase and frequency between the transport overhead and the SPE can be accommodated through pointer operations. The payload pointer, contained in H1 and H2 of the line overhead, designates the location of the J1 byte where the SPE begins.

If the frame rate of the SPE is too slow with respect to that of the transport overhead, then a positive stuff byte appears immediately after the H3 byte in the same frame containing inverted I bits in H1 and H2. Subsequent payload pointer is the previous pointer plus one and the new pointer shall remain constant for at least three frames.

If the SPE rate is too fast, then a negative stuff byte appears in the H3 byte in the frame containing inverted D bits. Subsequent payload pointer is the previous pointer minus one and the new pointer shall remain constant for at least three frames. Figure 2-7 shows the STS-1 overheads and pointer operations.

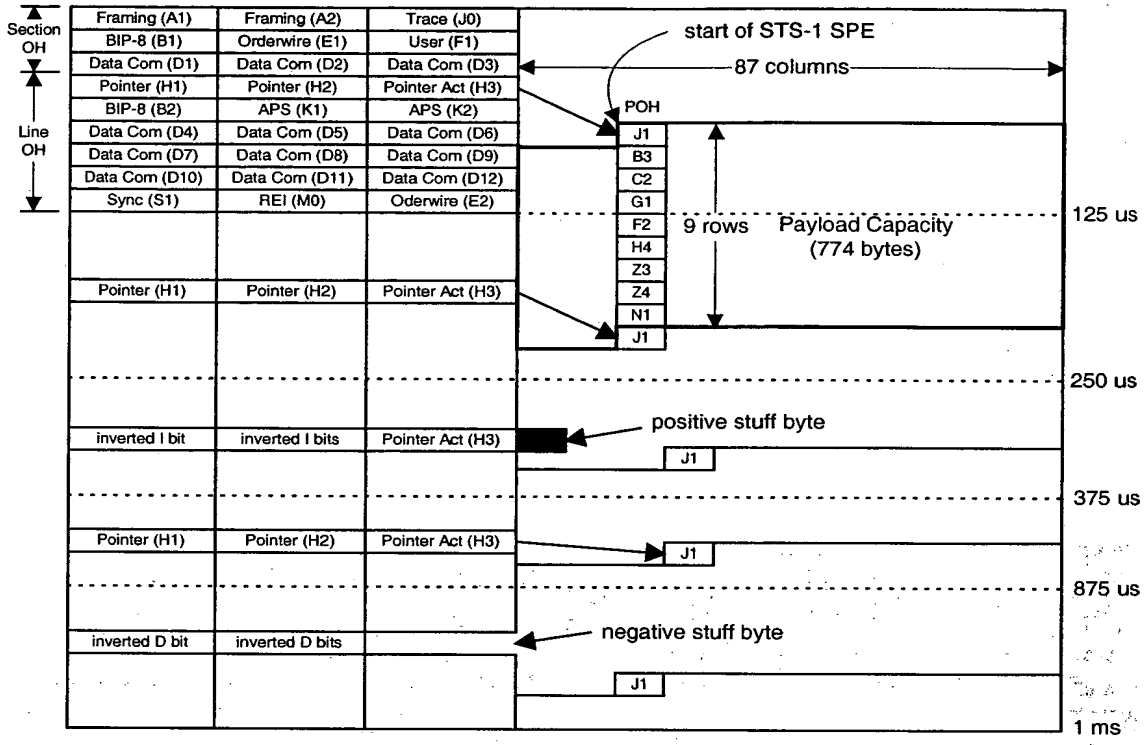

Figure 2-7. STS-1 Overheads and Pointer Operations

On a Vivace I/F module, the pointer operations take place in the PMC's SPECTRA (PM5315 or PM5316) chip. In the transmit direction, the TDM SAR marks the J0 (trace) and J1 bytes, in the AJ0J1 signal, for the SPECTRA to calculate both H1 and H2 bytes. The SAR also marks PJEs and NJEs, in the APL signal, for the SPECTRA to perform frequency justifications. In the receive direction, the SPECTRA provides the first SPE byte location (J1 byte) in the DJ0J1 signal and justification events (PJEs and NJEs) in the DPL signal.

3. ENCAPSULATION

3.1 TDM Packets

The TDM SAR in an ingress switch accepts STS SPEs as raw data and segments them into TDM packets. A TDM packet consists of a fixed number of overhead bytes and some payload bytes taken from the raw data. The TDM packet is transported over an MPLS network to a destination egress switch. The far-end TDM SAR then plays out the raw data. Figure 3-1 illustrates the encapsulation of end-to-end TDM packets over MPLS.

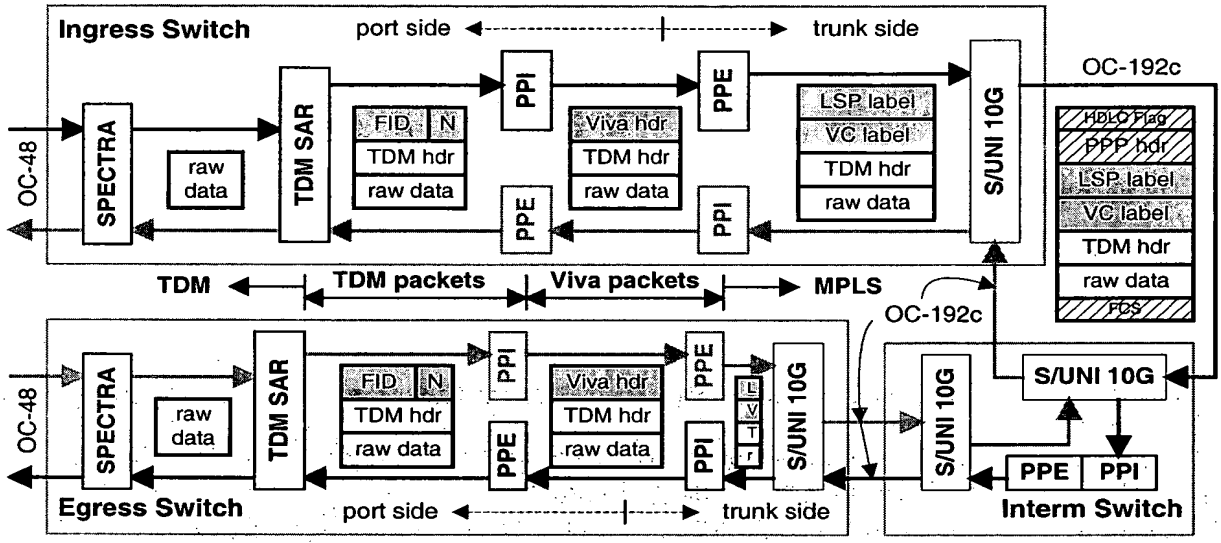

Figure 3-1. Encapsulated TDM Packet

At the ingress switch, a TDM SAR de-maps and segments OC-48 data streams into TDM packets. A TDM packet consists of a 22-bit flow ID (FID), a 10-bit payload size (N), a 32-bit TDM header, and N bytes of payload data. TDM packets from up to four TDM SARs are first processed by a packet parser in the ingress switch (PPI).

After processing, the PPI overwrites the 32-bit FID/N word with a Viva header to convert the TDM packet to a Viva packet. The Viva packets are further processed and passed to a trunk-side egress PP (PPE) within the switch. The PPE replaces each packet's Viva header with two MPLS labels: VC and LSP. The PMC S/UNI 10G takes the resulting MPLS packets from PPE and encapsulates them in HDLC-like PPP protocol to be transported in an OC-192c line.

S/UNI 10G in the intermediate switch delineates the packet boundaries using flag sequence detection, performs bit de-stuffing, and validates the FCS for each packet. The validated packet is sent through the PPI and PPE for label swapping. The label swapped packet is then re-encapsulated in PPP protocol by another S/UNI 10G and sent over an outgoing OC-192c line. This process repeats itself on each intermediate switch along the way until the packet reaches the egress switch.

At the egress switch, the encapsulation process is reversed. HDLC envelopes are removed and MPLS labels processed. The TDM packet, along with a 32-bit FID/N word, is sent to its TDM SAR for reassembly. Raw data in the TDM packet are extracted by the SAR and inserted onto an OC-48 line by a SONET payload aligner (SPECTRA).

3.2 HDLC-like PPP Packet

A TDM data stream is segmented into packets and encapsulated in HDLC frames. Each HDLC-like PPP packet has a 32-bit TDM header and at least two MPLS labels, as part of its information field, to associate the packet with the TDM stream. The HDLC envelope is added by a packet over SONET (POS) framer before the packet is transported on an OC-192c line. Figure 3-2 shows an encapsulated TDM packet.

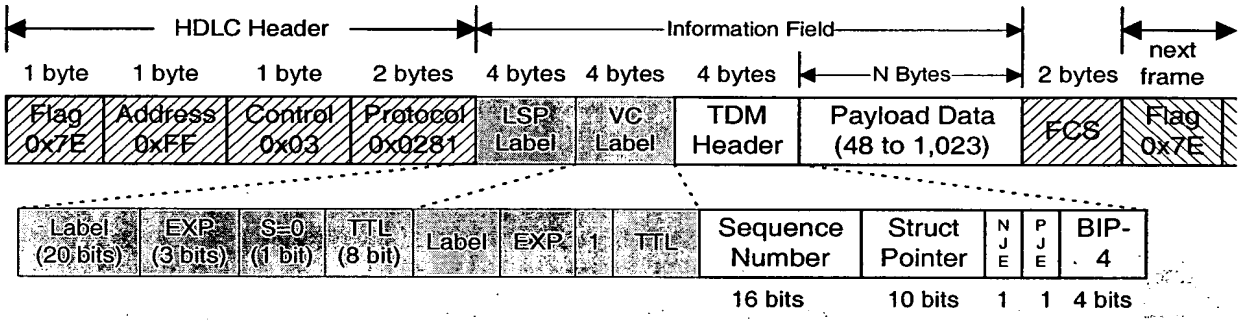

Figure 3-2. HDLC-like PPP Packet

A complete HDLC frame consists of 19 bytes of overheads and N bytes of TDM data. This frame size does not include bits inserted for synchronization or transparency (bit stuffing). The following provides a description for each field:

Flag Each frame begins and ends with an 8-bit flag, which binary sequence is 01111110 (0x7E in hex). Only one flag is required between two frames.

Address The address field is one byte in size and contains the all-stations address (0xFF), which will always be recognized and received.

Control The one-byte control field, which value is 0x03, identifies the packet as unnumbered information (UI) command with poll/final (P/F) bit cleared.

Protocol The protocol field is two bytes. Its value (0x0281) identifies the datagram encapsulated in the information field to be MPLS unicast.

MPLS Labels Each proposed MPLS label (LSP or VC) consists of a 20-bit label value, a 3-bit experimental use (EXP), a bottom of stack bit (S), and an 8-bit time to live (TTL). EXP bits may carry drop precedence. The S bit is set for the VC label to mark it as the last entry in the stack.

TDM Header The TDM header is 32 bits long and consists of the following fields:

Sequence Number The 16-bit sequence number cycles from 0 to 65,535.

Structure Pointer The structure pointer points to the J1 byte in the payload area. The value is from 0 to 1,022 with 0 means first byte after the TDM header. The pointer is set to 0x3FF (1,023) if a packet doesn't carry the J1 byte.

NJE/PJE NJE bit is set, with PJE = 0, for negative justification event. PJE bit is set, with NJE = 0, for positive justification event. The event is carried in five consecutive packets at near-end TDM SAR (transmitter). Far-end TDM SAR (receiver) plays out the event when three out of five packets with NJE or PJE bit set are received. If both bits are set, then path AIS event has occurred.

BIP-4 The bit interleaved even parity is over the first 28 header bits.

FCS The frame check sequence field is optional. If used, it calculated over all bits between the opening flag and the FCS, but not including bits inserted for synchronization or transparency.

3.3 Payload Capacity and Rate

The payload capacity of an OC-192c is 149,760 bytes per frame or 9,584.64 Mb/s. A number of STS-1, STS-3c STS-12c and STS-48c circuits may be emulated, with HDLC encapsulation, in an OC-192c line.

3.3.1 Emulate STS Circuits

An STS-1 SPE has 783 bytes per frame. The 783 bytes may be divided into 6.8684 blocks of 114 bytes each. The block size of 114 bytes is chosen so that the packet size, including a four-byte TDM header and up to 10 bytes of Viva header, is 128 bytes within the switch. When the Viva header is replaced with MPLS labels and the HDLC envelop is added, the packet size becomes 133 bytes (see Figure 3-2). Only one HDLC flag and two MPLS labels are included in the calculation. Therefore, the combined rate of 163 encapsulated SPEs is 163*6.868*133*8*8,000 = 9,529.6 Mb/s, which is within an OC-192c payload capacity.

An STS-3c SPE has 2,349 bytes per frame. The entire SPE may be divided into 5.4375 blocks of 432 bytes each. A Viva packet within the switch is therefore 446 bytes. Each HDLC frame becomes 451 bytes long. The combined rate of 61 encapsulated SPEs is 61*5.4375*451*8*8,000 = 9,573.8278 Mb/s, which can be fit in an OC-192c line.

An STS-12c SPE has 9,396 bytes per frame. The SPE may be divided into about 15.0577 blocks of 624 bytes each. An HDLC frame is 643 bytes. Only 15 SPEs, with combined rate of 15*15.0577*643*8*8,000 = 9,294.8166 Mb/s, may be fit in an OC-192c line.

Similarly, an STS-48c SPE may be divided into about 37.2857 blocks of 1,008 bytes each. Three SPEs, with combined rate of 7,352.1433 Mb/s, can be fit in an OC-192c line.

3.3.2 Example

About one of every seven STS-1 TDM packets has a valid structure pointer points to the beginning of the POH (J1 byte). About one of five STS-3c, one of 15 STS-12c, and one of 37 STS-48c packets has the valid pointer. The unused structure pointers are set to 0x3FF. Figure 3-3 shows six consecutive TDM packets of an STS-1 stream.

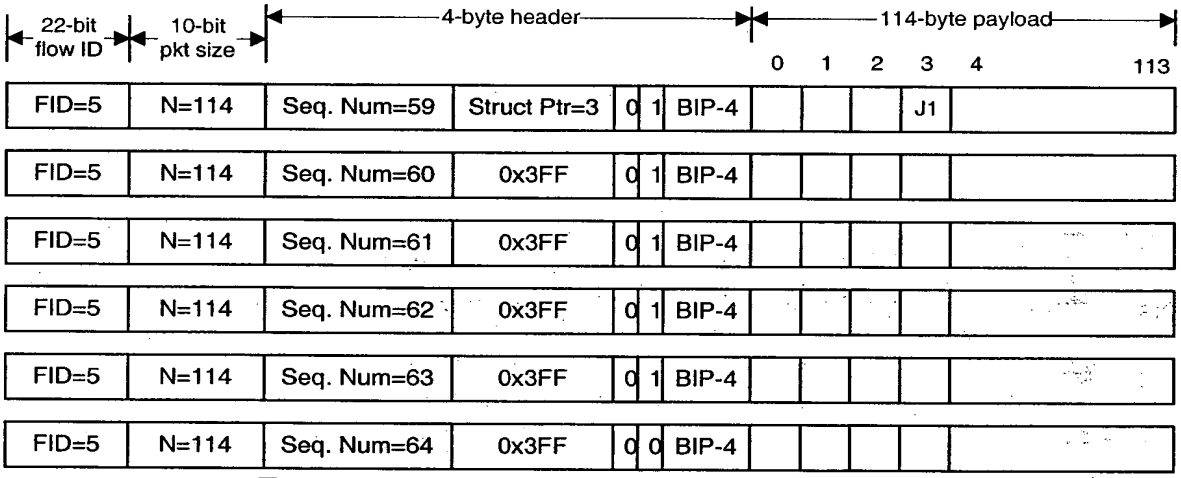

Figure 3-3 STS-1 SPE Data Blocks and Headers

The flow ID of each TDM packet is set to 5 and payload size (N) to 114 to indicate a flow #5 STS-1 TDM packet. Only the first packet, sequence number = 59, has a valid structure pointer points to the J1 byte in the payload area. Other pointers are invalid and set to 0x3FF. The STS-1 has a positive justification event in the frame and the PJE bit is set for five consecutive blocks from 59 to 63.

If the TDM circuit is in a path alarm indication signal (AIS) state, then both the PJE and NJE bits are set for the duration of the AIS state. In path AIS state, the structure pointer field is set to 0x3FF and all payload bytes are set to 0xFF. Other fields remain the same.

3.3.3 Summary

Table 3-1 summarized the block and HDLC frame size of various encapsulated TDM circuits. The block size is number of TDM data bytes. The HDLC frame size includes 19 bytes of overheads. The size of overheads is for reference only. Extra bits for HDLC synchronization and transparency purposes may be added to the overheads. This bit

stuffing may further reduce the payload capacity in an OC-192c (9,584.64 Mb/s) trunk line. The OC-48c trunk line, which has 2,396.16 Mb/s of payload capacity, is also listed for comparison.

TDM Circuit	Block/HDLC Frame Size (Bytes)	# Packets Per Second	Bandwidth Required (Mb/s)	Max # of Circuits / % in OC-48c	Max # of Circuits / % in OC-192c
STS-1	114 / 133	54,947.368	58.464	40 / 97.6%	163 / 99.43%
STS-1	242 / 261	25,884.297	54.046412	44 / 99.24%	177 / 99.81%
STS-3c	432 / 451	43,500	156.948	15 / 98.25%	61 / 99.89%
STS-3c	561 / 580	33,497.326	155.42759	15 / 97.3%	61 / 98.92%
STS-12c	624 / 643	120,461.53	619.6541	3 / 77.58%	15 / 96.98%
STS-12c	754 / 773	99,692.307	616.49722	3 / 77.19%	15 / 96.48%
STS-48c	1,008 / 1,027	298,285.71	2,450.7153	-	3 / 76.71%

Table 3-1. Summary of Various TDM Data Streams

There are two block sizes listed for an STS-1 SPE: 114 and 242 bytes. After adding the TDM and Viva headers, the size of a Viva packet becomes 128 or 256 bytes, which is a multiple of 64 bytes. The larger-size Viva packet (256 bytes) is more efficient in bandwidth use but has longer SAR delay.

Similarly, both the STS-3c and STS-12c circuits are listed with two block sizes each for comparison. Smaller block sizes (shaded rows), such as 114 bytes for STS-1, 432 bytes for STS-3c, and 624 bytes for STS-12c, are used in this document.

The size of an HDLC frame is the TDM block size plus total packet overheads (19 bytes). The total packet overheads consists of a four-byte TDM header, two four-byte MPLS labels, a four-byte PPP header, an HDLC flag, and a two-byte FCS. The HDLC frame size is used to calculate the bandwidth requirement of transporting a TDM circuit in a trunk line.

Entries in the "# Packets Per Second" column are calculated as SPE size per second (783*8,000 = 6,264,000 bytes for STS-1) divided by block size (114 bytes for STS-1). Entries in the "Bandwidth Required (Mb/s)" column are calculated as # packets per second times HDLC frame size (133 bytes for STS-1) times eight bits per byte. The last two columns list maximum number of TDM circuits that can be fit in an OC-48c or OC-192c line, along with their percent fill.